UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,850	12/20/2001	Eric J. Hansen	Hansen 1-1	3337

46900 7590 03/30/2005

STEVE MENDELSOHN
MENDELSOHN & ASSOCIATES, P.C.
1515 MARKET STREET, SUITE 715
PHILADELPHIA, PA 19102

EXAMINER	
WONG, LINDA	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,850	HANSEN ET AL.	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-10 and 12* is/are rejected.

7)☒ Claim(s) *2,4 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

   a. On page 3, paragraph [0036] and [0037], the label 804 is used for a noise-shaping loop. In Fig. 8, such a label is not included.

   Appropriate correction is required.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1, 3, 12** are rejected under 35 U.S.C. 102(e) as being unpatentable by Savelli et al (US Patent No.: 6441690).

   a. **Claim 1**, Savelli et al disclose a phase locked loop (PLL) configured to receive a reference signal (Fig. 2, label fref), a first data-modulated signal based on the input data signal (Fig. 2, input to label 30, path consisting of label 3, 32, 38, 40 and 42) and apply the first data-modulated signal to a voltage controlled oscillator (VCO) (Fig. 2, label 1), a second data-modulation path configured to generate a second data-modulated input signal based on the data signal (Fig. 2, path consists of labels 30, 32, 36, 9, and 8) and applies the second data-modulation path to a frequency divider. (Fig. 2, labels 9 and 8)

   b. **Claim 3**, Savelli et al disclose a PLL comprised of a phase detector, a loop filter connected to the phase detector (PD) and VCO and a frequency divider

connected to the VCO and PD through a feedback loop. (Fig. 2, labels 7, 5, 1, 8)

c. **Claim 12**, Savelli et al disclose a first data-modulation path comprised of a Gaussian filter (label 30) coupled to a digital-to-analog converter (DAC) (label 40) coupled to a VCO (label 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 5, 6, 8, 9** are rejected under 35 U.S.C. 103(a) as being unpatentable Savelli et al (US Patent No.: 6441690) in view of Perrott et al (US Patent No.: 6008703).

a. **Claim 5**, Savelli et al discloses a PD (Fig. 2, label 7) generates a phase different signal based on a reference signal (Fig. 2, label fref) and frequency divider (Fig. 2, label 8), a loop filter (Fig. 2, label 5) configured to generate a loop-filtered signal based on the frequency-divided signal from the PD (Fig. 2, labels 8 and 5), a VCO generating an output based on the first data modulated signal (Fig. 2, input from label 42) and loop-filtered signal (Fig. 2, output from label 5), a frequency divider (Fig. 2, label 8) generating a frequency-divided signal based on the output from the VCO (Fig. 2, label 8 and 1) and a second data modulated input signal (Fig. 2, label 9). Although Savelli et al does not

disclose that the second data-modulated signal determines a division factor, Perrot et al discloses a second data-modulated input signal determines the frequency divider factor (Col. 7, line 47-49) applied to the frequency divider. It would be obvious to one skilled in the art to use the second data-modulated signal as a division factor as opposed to a predetermined factor, N, as disclosed by Savelli et al to reduce any degree of a high frequency signals for better synchronization of the low frequency found in the PLL.

a. **Claim 6**, Perrott et al discloses a digital sigma-delta modulator configured to generate the second data-modulated input signal. (Fig. 2A, labels 56 and 58)

b. **Claim 8**, Perrott et al discloses a Guassian frequency shifted keyed modulation and the input data signal is Gaussian low-pass filtered (Fig. 2A, label 46) prior to the first modulation path. Although Perrott et al does not disclose a second modulation path, Jorgensen discloses a second modulation path filtered by a Guassian filter (Fig. 1, label 9). It would be obvious to one skilled in the art to add a second data-modulation path to Perrott et al's invention to generate modulated output with a frequency within the PLL bandwidth.

c. **Claim 9**, Perrott et al discloses a sigma-detla modulator quantizes noise or spurious signals to high frequencies which are attenuated by the PLL. (Col. 8, lines 7-14 and lines 39-54)

2. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable Savelli et al (US Patent No.: 6441690) in view of Perrott et al (US Patent No.: 6008703) and further in view of Riley (US Patent No.: 6822488).

   a. **Claim 7**, Riley discloses a frequency synthesizer operating with two or more different reference signals (Fig. 3, label 16). Although Riley does not disclose a second data-modulation path, Perrot et al discloses a digital compensation and transmit filtering that adjusts the gain of the modulated signal to be higher than the frequency of the PLL (Col. 3 and 4, lines 66-67 and 1-4) and a carrier selection block injecting a carrier frequency (Fig. 2, label 54) based on the output from modulated signal. It would be obvious to one skilled in the art to allow a selection from multiple reference signals disclosed by Riley to allow synchronization of more than one signal of different frequencies.

Allowable Subject Matter

3. **Claims 2, 4, 10 and 11** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LW

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600